**Amendments to the Specification**

Please replace the title of the patent application with the following amended title

~~SEMICONDUCTOR DEVICES AND METHODS OF FABRICATING THE SAME~~

METHODS TO REDUCE STRESS ON A METAL INTERCONNECT

Please replace paragraph [0003] with the following amended paragraph:

**[0003]** In the prior art, the passivation layer has, in some instances, been fabricated by depositing a Plasma Enhanced-Tetra-Ethyl-Ortho-Silicate (PE-TEOS) oxide layer using a Plasma Enhanced Chemical Vapor Deposition (PECVD) on a semiconductor substrate on which an uppermost metal interconnect for the semiconductor device has been formed, and subsequently depositing a $SiH_4$ nitride layer using PECVD. Also, the passivation layer has been fabricated by depositing a $SiH_4$ oxide layer using a high density plasma Chemical Vapor Deposition (HDPCVD) process and subsequently ~~depositinga~~ depositing a $SiH_4$ nitride layer using PECVD.

Please replace paragraph [0012] with the following amended paragraph:

**[0012]** The aluminum oxide layer 105 is a kind of $Al_xO_y$ layer formed on the aluminum layer 104. The ~~AlxOy~~ $Al_xO_y$ layer is formed by performing a plasma treatment to the aluminum layer 104 using $N_2O$ or $O_2$ gas and annealing the treated layer in an atmosphere of inert gas, such as Ar or He, or of gas, such as $N_2O$, $O_2$, $N_2$ or $H_2$, etc. at a low temperature of, for example, 200 to 400. for 10 to 100 minutes.

Please replace paragraph [0020] with the following amended paragraph:

**[0020]** Since the stress-relief layer 105 has a high hardness characteristic and a low stress susceptibility relative to the metal interconnects 102, the ~~stress-releif~~ stress-relief layer 105 serves to relieve stress for the metal interconnects 102. Formation of the stress-relief layer 105 prevents cracking during a subsequent packaging process, so that leakage current of the semiconductor device may be reduced and the breakdown voltage thereof may be increased.